

UPGRADE OF THE TRIGGER SYNCHRONISATION AND DISTRIBUTION SYSTEM OF THE BEAM DUMPING SYSTEM OF THE LARGE HADRON COLLIDER

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Abstract

Various upgrades were performed on the Large Hadron Collider (LHC) Beam Dumping System (LBDS) during Long Shutdown 1 (LS1) at CERN, in particular to the Trigger Synchronisation and Distribution System (TSDS): A redundant direct connection from the LHC Beam Interlock System to the re-trigger lines of the LBDS was implemented, a fully redundant powering architecture was set up, and new Trigger Synchronisation Unit cards were deployed over two separate crates instead of one. These hardware changes implied the adaptation of the State Control and Surveillance System and an improvement of the monitoring and diagnosis systems, like the various Internal Post Operation Check (IPOC) systems that ensure that, after every beam dump event, the LBDS worked as expected and is ‘as good as new’ for the next LHC beam. This paper summarises the changes performed on the TSDS during LS1, highlights the upgrade of the IPOC systems and presents the problems encountered during the commissioning of TSDS before the LHC Run II.

INTRODUCTION

LHC Beam Dumping System

The Large Hadron Collider (LHC) Beam Dumping System (LBDS) is responsible for the single turn extraction of the beam from LHC rings, after reception of a Dump Request (DR). It is composed, for each beam, of 15 extraction kicker magnets (MKD) followed by 15 extraction septum magnets (MSD) to extract the beam from the ring, followed by 10 dilution kicker magnets (MKB) in the extraction channel to spread the beam over the dump target (TDE) surface [1].

Each MKD and MKB is powered by a High-Voltage Pulsed Generator (HVPG), to produce the fast high current pulse needed to extract and dilute the beam, upon reception of a trigger.

Trigger Synchronisation and Distribution System

Within the LBDS control architecture, the Trigger Synchronisation and Distribution System (TSDS) is responsible for the detection of a DR from various sources, the subsequent generation of a dump trigger synchronised with the beam-free abort gap of the LHC, and the distribution of this Synchronous Beam Dump Trigger (SBDT) to the 25 HVPG of the 15 MKD and 10 MKB [2]. The TSDS is built around a major component, the Trigger Synchronisation Unit (TSU), which detects the DR from sources like the Beam Interlock System (BIS) [3], the State Control and Surveillance System (SCSS) [4], the Beam Loss Monitor Direct Dump

(BLMDD), and issues a dump trigger synchronised with the Beam Revolution Frequency (BRF) signal [5].

The TSDS also includes an asynchronous Re-Triggering System (RTS) to cover the cases where the SBDT is not distributed properly, or when a MKD HVPG self-triggers [2].

During the LHC Run I operation, all beam dump requests were properly detected and distributed. Nevertheless some weaknesses of the TSDS were pointed out during various reviews and discussions, and a consolidation project was planned for Long Shutdown 1 (LS1).

Re-Trigger System Principle

The RTS is entirely passive and is composed of two redundant floating Re-Trigger Lines (RTL). A simplified view of one RTL is shown in Fig. 1. The 25 HVPG are interconnected by a chain of Re-Trigger Boxes (RTB), connected serially using a twisted pair cable. These RTB are composed of simple insulation transformers and decoupling diodes. When an HVPG triggers, five internal pickups in the HVPG will inject pulses in the RTL through five input transformers of the RTB. These pulses are then transmitted to all the other HVPG through two output transformers in each RTB. Thanks to this mechanism, in case of self-trigger of one MKD HVPG, all the other HVPG of LBDS will be triggered automatically as quickly as possible. Only the 15 MKD HVPG will inject pulses in the two RTL, as MKD see the circulating beam, and a self-trigger of one MKD HVPG requires retriggering all LBDS HVPG. The MKB HVPG do not inject pulses in the two RTL, because MKB do not impact the circulating beam, but a self-trigger of MKB HVPG will be detected by the various surveillance systems and a normal SBDT will be issued.

To cover a possible failure of the distribution of the SBDT issued by the TSU, an asynchronous dump trigger is also systematically generated by the TSU at the time it detects a DR. As up to 90 μ s (one beam revolution) may be necessary for the TSU to issue a synchronous dump, the asynchronous dump trigger is delayed by 250 μ s and injected in the RTL using a Trigger Delay Unit of 250 μ s (TDU-250), as can be seen in Fig. 1.

The upgrades performed on the various TSDS sub-systems, along with their motivations, are detailed in the following sections.

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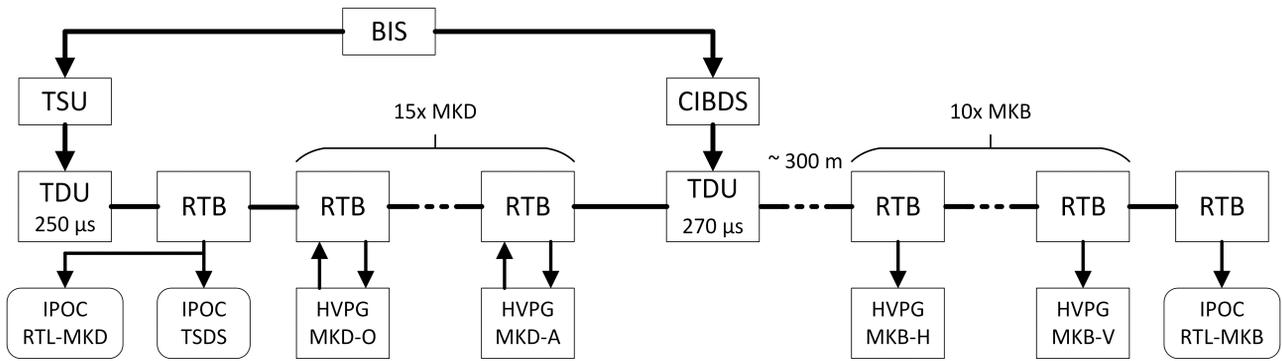


Figure 1: Simplified view of one Re-Trigger Line.

UPGRADES TO TSDS

Improvement of Power Distribution Architecture

During LHC operation in 2012, we faced an unexpected event: One Power Supply Unit (PSU) of one of the Front-End Computers (FEC) located in the control electronics racks of the LBDS failed, causing a short-circuit on its main input. The circuit breaker located in the distribution bar for the electronics rack did not react quickly enough, and the short circuit propagated up to the general circuit breaker in the UPS distribution powering the LBDS. This resulted in eight racks of electronics losing their UPS, which was totally unexpected for such a simple FEC PSU failure. The LBDS nonetheless properly executed a synchronised beam dump, but some of the diagnosis systems were not available for post-operation analysis. An internal review of LBDS powering was conducted later in 2012, when recommendations for a consolidation of power distribution during LS1 were given.

To avoid such a situation in the future, we provided a distribution box to power each crate PSU through an individual circuit breaker, as depicted in Fig. 2.

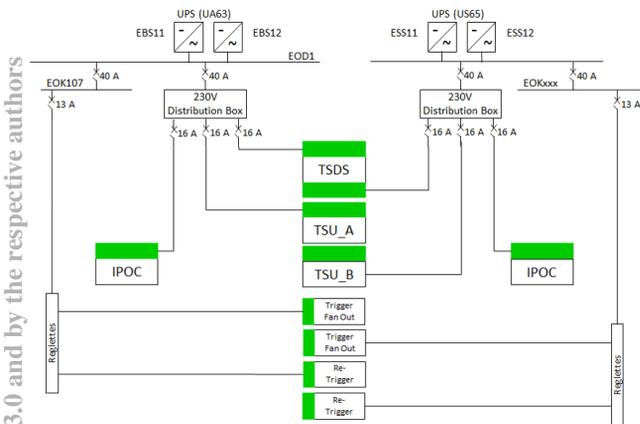


Figure 2: Full redundant electrical distribution.

During LS1, a new dedicated direct connection to a second UPS was also provided for LBDS, so now two independent UPS, one located in UA63, the other in US65, power the various LBDS redundant PSU, see in Fig. 2.

The UPS system was also upgraded during LS1, and a new fully redundant architecture was implemented. As illustrated by Fig. 3, a third 'backup' UPS unit was installed to feed the bypass line of the first two UPS units. Hence, in case of failure of one of the first UPS units, the backup unit guarantees the redundancy of the UPS distribution paths.

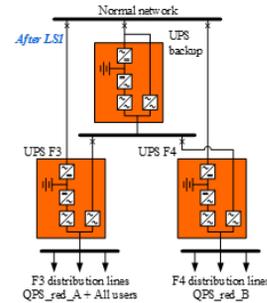


Figure 3: Full redundant UPS configuration.

All the FEC housing critical post-operation diagnosis systems were equipped with two redundant PSU, each connected to a different UPS. The monitoring of the state of all the redundant PSU of the LBDS crates is now performed remotely through Ethernet, so a software interlock system can request a beam dump in case a failure is detected in a PSU.

Before the startup of LHC Run I, a simulation of UPS failure was performed for LBDS. Each of the two UPS was disconnected, in two successive tests. Some non-conformities were detected, such as two redundant PSU of a FEC connected to a same UPS. These problems were fixed, but the UPS test proved to be useful and subsequently shall be planned after every intervention on the LBDS power distribution.

New Deployment of TSU Cards

During the LHC Run I operation, a new failure mode of TSDS was identified: Due to the deployment of both TSU cards in the same TSDS VME crate, along with the BRF optical receiver card and the BLMDD interface card, if only the +12V VME power is lost, neither synchronous nor asynchronous triggers are issued. This power failure was not detectable and would have caused the LBDS to not

function, which is totally unacceptable. This failure never occurred, but at the time the failure mode was identified, we immediately requested a beam dump and stopped the LHC operation until a solution was found. The same day, we implemented a surveillance of the +12V power supply of the TSDS VME crate, to inject an asynchronous trigger on the RTL in case a failure is detected.

In order to definitively remove this +12V common failure mode, a new deployment of the two TSU cards was performed during LS1. Each TSU is now installed in its own VME crate with a redundant PSU, and a third TSDS VME crate contains the RF optical receiver card and the BLMD interface card, as can be seen in Fig. 2.

Design of a New TSU Card

Following an external review of the TSU card design performed in 2010 during which recommendations for minor hardware improvements were made, and due to the new deployment of TSU cards over two separate crates, a new TSU card was developed.

A new cabled interconnection between the two boards was implemented to replace the common VME backplane. A surveillance of all internal voltages was added to the TSU card itself, and a DR is issued to the redundant card in case any power supply failure is detected. Additionally, an internal continuous surveillance of the CRC of the TSU programmable logic circuits (FPGA) was implemented, so in case of a Single Event Upset corruption of one of the programmable circuits, an incorrect CRC is detected and a DR is issued to the redundant TSU.

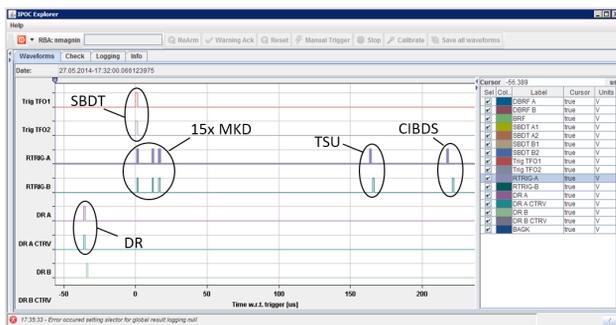


Figure 4: View of some signals captured by IPOC-TSDS.

Numerous on-board post-operation diagnosis functionalities have been added, such as the surveillance of the output current of the SBDT signals. Additionally, 32 TSU internal signals are now acquired and analysed by an Internal Post Operational Check (IPOC) system [6], such as all the redundant dump requests from the various clients, which are checked for presence and correct synchronisation after every dump. A view of some signals captured by this IPOC-TSDS is shown in Fig. 4. The eXternal Post Operation Check (XPOC) system [7] receives the results of IPOC-TSDS analysis after every dump, and will inhibit the injection of beam in LHC in case any problem is detected after the last dump execution.

Direct Connection from the BIS to the RTS

It was noted that the LBDS is very sensitive to any unidentified failure mode of the TSDS. Despite the large redundancy within them, in case of simultaneous failure of both TSU cards, no beam DR would be executed. To reduce this sensitivity, a direct link has been established between the BIS and the RTS of the LBDS [3]. This new link consists of a new electronic board (CIBDS) that follows the same principle as the TSU: It is included in the BIS optical loops, and generates an asynchronous dump trigger when it detects an opening of the beam permit loop. This additional asynchronous trigger is delayed by 270 μ s and injected in the RTL, between the MKD and MKB RTB, using a TDU of 270 μ s (TDU-270), as displayed in Fig. 1.

To assess whether the addition of this new hardware has a significant negative impact on the overall rate of false beam dumps of the LBDS, a reliability study of the CIBDS card and the TDU was carried out, and revealed that the increase in failure rate is almost negligible [8].

Adaptation of the SCSS

First, the SCSS hardware and software were updated to add the functionalities for the surveillance of all the power supplies of TSDS, as explained above. In case a power supply failure is detected, a beam dump is requested before the situation further deteriorates. Secondly, the CIBDS card got a direct redundant connection to the SCSS to inhibit the CIBDS pulses on the re-trigger lines when the LBDS is in local test mode, to make sure that any activity on the BIS does not interfere with LBDS tests. A read-back of the inhibit status of the CIBDS was also implemented, and a beam dump is requested if the CIBDS is not detected as operational [3] Finally, an improvement to the SCSS was the implementation of a 'spontaneous triggering' test, to make sure that the re-trigger line is working as expected, and that all HVPG are triggered in case one of them triggers spontaneously. The SCSS will send a trigger to all MKD HVPG one after the other on a dedicated line, to simulate a MKD HVPG spontaneous trigger and check that all other HVPG are triggered through the re-trigger line as expected. This system is only active when the LBDS is in local test mode.

Check of Re-Trigger Lines Continuity

The RTL is actually composed of two twisted pairs, one to transmit the re-trigger pulses and the other to allow the SCSS to check that the line is closed using a DC current. During the first tests with CIBDS, we faced an unforeseen problem: The RTL was physically closed and the DC current was normal so the SCSS did not detect any error, but the CIBDS re-trigger pulse was not visible on the IPOC-TSDS for one RTL (See Fig. 4). Further investigations showed that a pin was not connected within one of the 110 connectors included in one RTL. We then realised that the DC current loop continuity did not guarantee the continuity of the re-trigger pulse line. Such a fault could not be detected before

LS1, because the IPOC-TSDS picks up the signal on the RTL using a RTB placed at the output of the TDU of the TSU, at the MKD extremity of the line, as shown in Fig. 1. This non-conformity was detected thanks to the addition of the CIBDS, and the check by IPOC-TSDS of the presence of CIBDS re-trigger pulse travelling through the RTB of the 15 MKD. However, with only one IPOC-TSDS system at the MKD extremity of the re-trigger line, we cannot ensure that the re-trigger pulses reach the MKB extremity of the line, so a new IPOC system was added at the MKB extremity of the RTL, to capture and check the presence of the two re-trigger pulses from the TSU and CIBDS cards.

Problem of Re-Trigger Lines Absorption

During the re-commissioning of the RTL, we were very surprised to see that the CIBDS re-trigger pulse was not detected by the IPOC-TSDS system when pulsing at energies above 3 TeV. After further investigations, we discovered that the CIBDS pulse underwent an attenuation that increased with both the LBDS energy and the delay between the SBDT and CIBDS pulses. The CIBDS pulse is sometimes so low at the input of the IPOC-TSDS that it is not detectable by its binary digitiser (TTL). We added a new IPOC system at the MKD extremity of the RTL, in parallel with the existing IPOC-TSDS, but with high resolution digitisers, as displayed in Fig. 1.

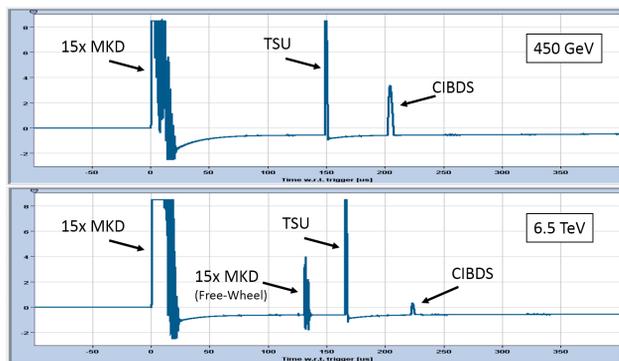


Figure 5: IPOC-RTL-MKD at 450 GeV and 6.5 TeV.

Figure 5 shows an acquisition of this new IPOC-RTL-MKD for a pulse at 450 GeV, and another at 6.5 TeV. We first see the pulse train injected by the 15 MKD HVPG when they receive the SBDT, then later the TSU re-trigger pulse, and finally, the CIBDS re-trigger pulse, which has an acceptable level at 450 GeV, but a very low level at 6.5 TeV, making its detection very difficult.

This problem of re-trigger pulse attenuation is not yet fully understood. A project was started to simulate the behaviour of the whole RTL in order to understand the phenomenon, and find a way to reduce this attenuation.

Change of TDU Delay

A pulse due to a free-wheel pickup inside the 15 MKD HVPG appears on the RTL when operating above 5 TeV, see Fig. 5. In some cases, this pulse could occlude the TSU

re-trigger pulse, and thus hinder IPOC from checking its presence. This was not an issue during LHC Run I, as the LHC energy was limited to 4 TeV. To avoid this problem, we changed the TDU delay of TSU and CIBDS from respectively 200 and 250 μ s to 250 and 270 μ s.

CONCLUSION

Although the TSDS performed as expected during LHC Run I, some major problems were discovered, and an important number of improvements were implemented during LS1. Many diagnosis systems were added, and already proved to be useful, as they highlighted various issues with the re-trigger lines during the re-commissioning phase. A problem of re-trigger pulses attenuation is still not fully understood, and a full simulation of the re-trigger lines behaviour has been launched in order to address it. The TSDS was successfully commissioned and has been operating flawlessly since the start of LHC Run II.

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