# THE POWER SUPPLY CONTROL SYSTEM OF CSR

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*Abstract*

This article gives a brief description of the power supply control system for Cooler Storage Ring (CSR). It introduces in detail mainly of the control system architecture, hardware and software. We use standard distributed control system (DCS) architecture. The software is the standard three-layer structure. OPI layer realizes data generation and monitoring. The intermediate layer is a data processing and transmission. Device control layer performs data output of the power supply. We use ARM + DSP controller designed by ourselves for controlling the power supply output. At the same time, we have adopted the FPGA controller designed for timing for power supply control in order to meet the requirements of accelerator synchronizes the output of the power supply.

## INTRODUCTION

HIRFL-CSR, a new ion Cooler-Storage-Ring (CSR) project, is the post-acceleration system of the Heavy Ion Research Facility in Lanzhou (HIRFL). HIRFL-CSR is a multi-purpose CSR system that consists of a main ring (CSRm), an experimental ring (CSRe), and a radioactive beam line (RIBLL II) to connect the two rings. Figure 1 show an Overall Layout of HIRFL-CSR [1]. The two existing cyclotrons SFC (K = 69) and SSC (K = 450) of the HIRFL will be used as its injector system. The heavy ion beams with the energy range of 8–30 MeV/u from the HIRFL will be accumulated, cooled and accelerated to the high-energy range of 100–400 MeV/u in the main ring, and then extracted fast to produce RIB or highly charged heavy ions. The secondary beams (RIB or highly charged heavy ions) will be accepted and stored by the experimental ring for many internal-target experiments or high-precision spectroscopy with beam cooling. On the other hand, the beams with the energy range of 100–900 MeV/u will also be extracted from CSRm by using slow extraction or fast extraction for many external-target experiments.

Two electron coolers located in the long-straight sections of CSRm and CSRe, respectively, will be used for the beam accumulation and cooling. One internal target in the long-straight section of CSRe will be used for nuclear physics and highly charged state atomic physics, and many external targets of CSRm will be used for nuclear physics, cancer therapy study and other researches.

CSR is a double ring system. In every operation cycle, the stable-nucleus beams from the injectors are accumulated, cooled and accelerated in the main ring (CSRm), then extracted fast to produce RIB or highly charged ions. The experimental ring (CSRe) can obtain the secondary beams once for every operation cycle. The accumulation duration of CSRm is about 10 s. considering the ramping rate of magnetic field in the dipole magnets to be 0.1–0.4 T/s, the acceleration time of CSRm will be nearly 3 s. Thus, the operation cycle is about 17 s [2].

In CSRe, two operation modes will be adopted. One is the storage mode used for internaltarget experiments or high-precision spectroscopy with electron cooling. Another one is the deceleration-storage mode used for atomic-physics experiments.

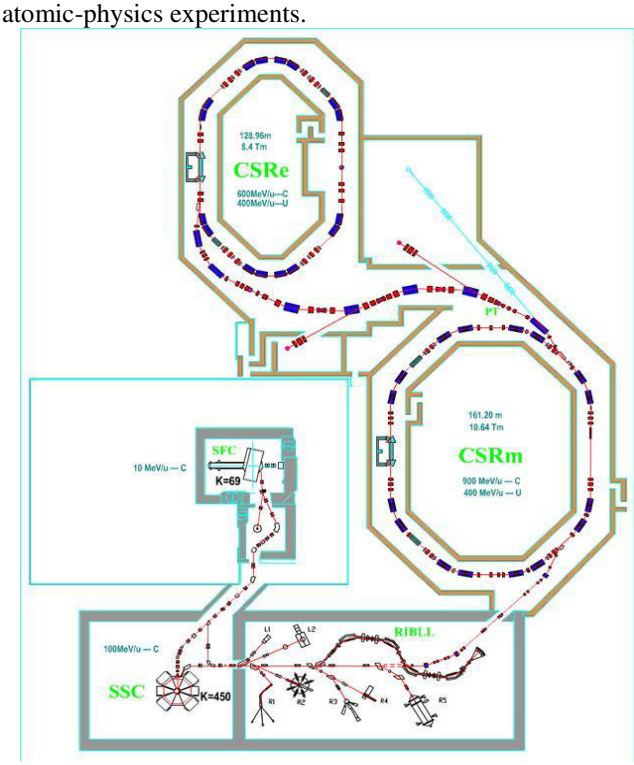


Figure 1: Overall Layout of HIRFL-CSR.

## SYSTEM INTRODUCTION

The control system is based on the Ethernet star topology. It takes Ethernet as the transmission medium to connect each part, mainly including: database system, the synchronization server, the front end server, the I/O part (ARM controller and the DSP processor) and the communication module. Database system and synchronization server is the information and control centre of the whole system. There is an independent Ethernet connection between the front end of the server and the I/O component, and a front-end server manages multiple I/O components. The I/O part directly controls the device object, and an I/O part controls one or four device objects. The structure of the power control system is shown in Figure 2. In the system, power control is accomplished by three kinds of data files: process data, event table data and command table data.

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In the power supply control system, the ARM controller is directly used as a network node to realize the information exchange between the upper control centres; at the same time, the DSP control board is used as the control unit, and the real-time and accurate monitoring of the control equipment is carried out.

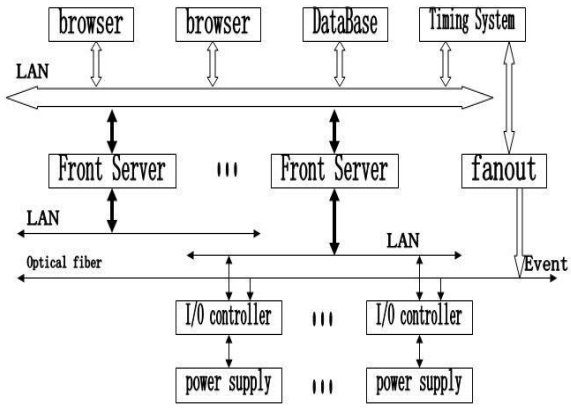


Figure 2: The structure of the power control system.

## HARDWARE

There are two types of hardware for the control system. The specific contents are as follows:

### *The ARM Controller*

The ARM controller with S3C4510B as the core, connects DSP through the back, and is provided by a power supply for the backing plate. The structure of the ARM controller is shown in Figure 3.ARM controller with SDRAM, Flash, data CPLD and system Flash. It receives data files (process data, event data, and command table data) through the network; Data transmission to the DSP through the HPI port of DSP; System Flash for curing u-boot, kernel and root file system; Data Flash is used to store the important control parameters and waveform data, so as to avoid the loss of data.

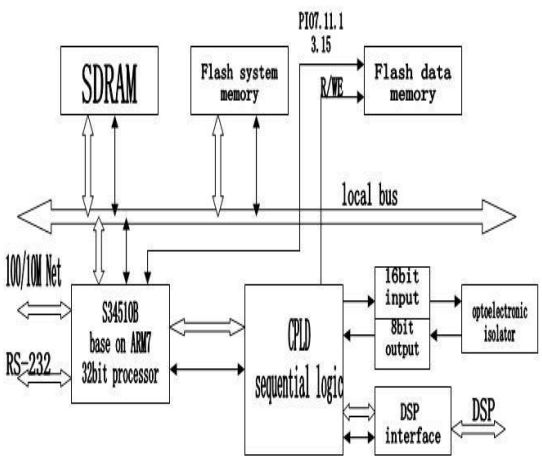


Figure 3: The structure of the ARM controller.

### *The DSP Processor*

The DSP processor is connected to the ARM controller by the backing board, and the power supply is provided by the backing plate. The structure of the DSP processor is shown in Figure 4.It takes TMS320VC5402 as the core, and the SRAM and Flash of 512K*16bit. Through the back board, the DSP processor receives the process data and event data from the HPI port of the ARM controller, and stores it in the SRAM. The trigger event is received by the FPGA case of a light switch. Flash used to cure DSP programs and procedures. The DSP processor has a DAC and an ADC channel [3].

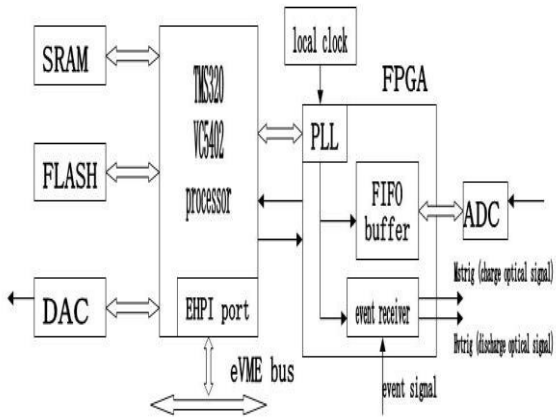


Figure 4: The structure of the DSP processor.

## SOFTWARE DESIGN

The power supply control system uses the C/S structure. The structure of the software is shown in Figure 5.The first layer is a synchronization server. It is through the data exchange with the database system to get the accelerator's effective operation data and distribution, and also provides the time system of the trigger event and customer operation procedures. Database service is second layer. It provides the synchronization data file required by the CSR to run an independent cycle. A network connection is used between the synchronous server and the I/O component and the database system.

The software mainly includes: the Oracle database, the embedded database on the server, the application program and the service program of the related peripheral driver, the waveform algorithm program of the front generator. In addition to the Web based debugging interface program and synchronous trigger program, the rest of the software is a server program or automatic implementation of the application, without user intervention.





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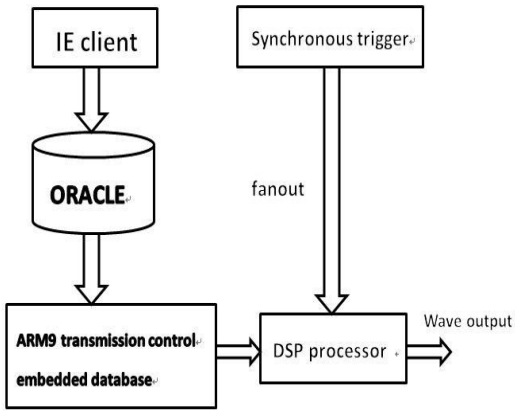


Figure 5: The structure of the software.

We provide a web interface program based on Web technology, which can be easily loaded into the Oracle database in the front end of the binary waveform file. The waveform data is passed to the database file of the front controller by update command and the IP address of the initial set of the front-end controller, at the same time to inform the embedded database SQLite has a new data to arrive. The embedded database stores the new data according to the distribution of the DSP storage space and the current waveform output buffer. When the required data is passed to the DSP storage space, we can start the pulse trigger program to generate the optical pulse signal. After the trigger event is consistent, the DSP processor outputs the waveform. The waveform data download flow chart is shown in Figure 6.

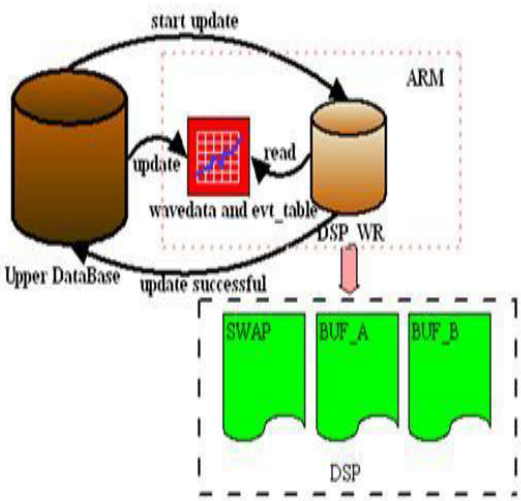


Figure 6: The waveform data download flow chart.

## SUMMARY

The control system has been applied to the actual operation in 2008 and passed the acceptance of the CSR expert group. It implements the requirements of the power supply control system for the CSR project. The control system has been stable operation of the seven-and-a-half years, and ensures the normal conduct of the experiment.

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