History and Future of the Machine Protection System from the High Intensity Proton Accelerator (HIPA)

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Introduction

HIPA has been in operation for more than 40 years. During this time the accelerator setup has been continuously growing and changing. The beam current has increased by a factor of 24 since the beginning, today reaching 2.4mA (@ 590MeV). This places increasing demands on our Machine Protection System (MPS) which must remain scalable and easy to maintain. A program of continuously ongoing upgrade tasks is necessary to replace aging electronics with state of the art technology to support the next generation of operation.

The MPS concept is of an independent running system which is integrated into the control system. All safety relevant signals are collected from along the beamline. In the case of one illegal input state the beam switch-off command must be propagated towards the source of the proton beam where finally the beam gets deflected by a fast kicker magnet.

Past

In the past decades different technologies have been used for the MPS. The previous generation before the current one was CAMAC based. The CAMAC Loop Controller was connecting multiple crates in a serial loop with the control system. Over this Serial Dataway the MPS modules (figure 1) in the crates were directly accessible.

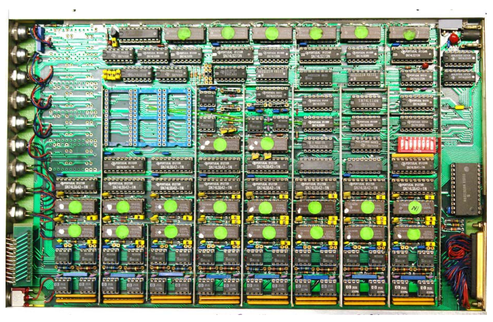

figure 1: CAMAC MPS module.

The MPS modules were a PSI development, where the internal logic was realized with EPROM's (figure 2). Adding new modules and keeping the logic and hardware documentation up to date took a lot of resources.

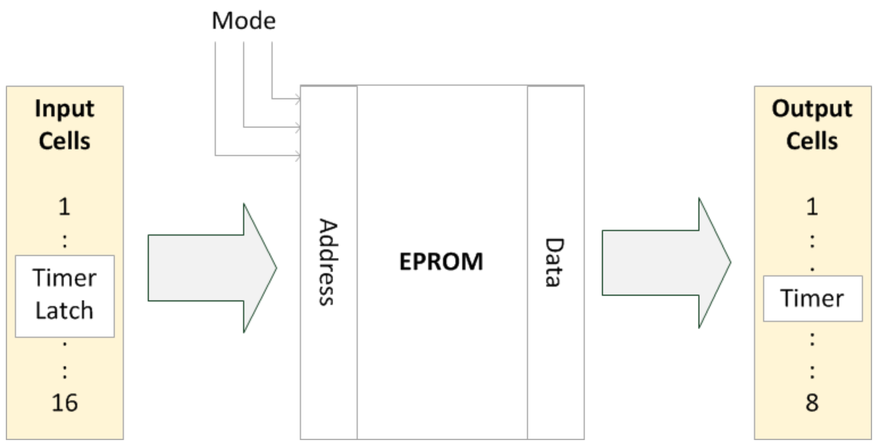

figure 2: Principle for logic decoding with EPROM.

Present

With the decision in 2007 to replace the CAMAC Crates with VME Crates the MPS modules got upgraded too. The failure detection logic was moved into FPGA's which increased the speed and added the possibility to realise more complex functions. For this purpose the MPS modules were implemented on an Industry Pack (IP) form factor (figure 3) to fit on a VME Carrier Card (4 IP's per card).

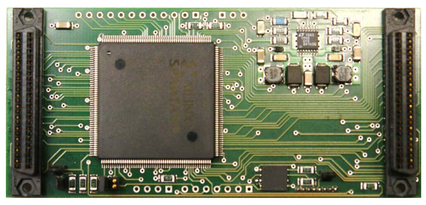

figure 3: Industry Pack MPS module.

The connection between the individual FPGA's is established on the digital dual current loop principle to detect faulty or missing links. The current design includes optical galvanic Isolation to protect the electronics.

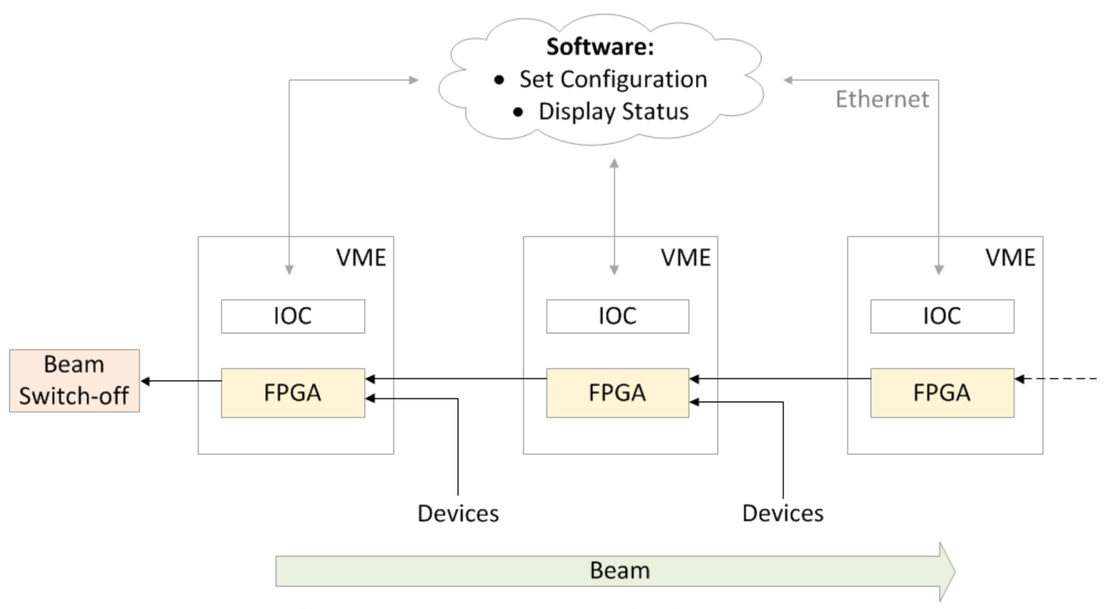

figure 4: MPS Structure in the Control System.

Future

The concept for the next generation MPS is a VME based board design with a single FPGA. All VME Slot I/O's will be connected to the FPGA and a modular firmware design will lead to improved efficiency (in I/O usage) and flexibility. Fewer module interconnections are needed which frees resources for devices and also will result in reduced cabling. Hardware costs will be reduced and the ability to update the firmware over VME will make maintenance easier. Updating the I/O electronics to CMOS technology and GMR galvanic isolation will decrease the power consumption and extend the board lifetime. A high speed link should make a topology change possible and simplify the physical cabling.

CAMAC:	A modular Instrumentation System for Data handling.
IOC:	Input Output Controller, Single Board Computer used as host in the VME Crate.
VME:	Versa Module Eurocard
GMR:	Giant Magneto Resistive

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