MOPGF134

DESIGN OF FAST MACHINE PROTECTION SYSTEM FOR THE C-ADS INJECTION I

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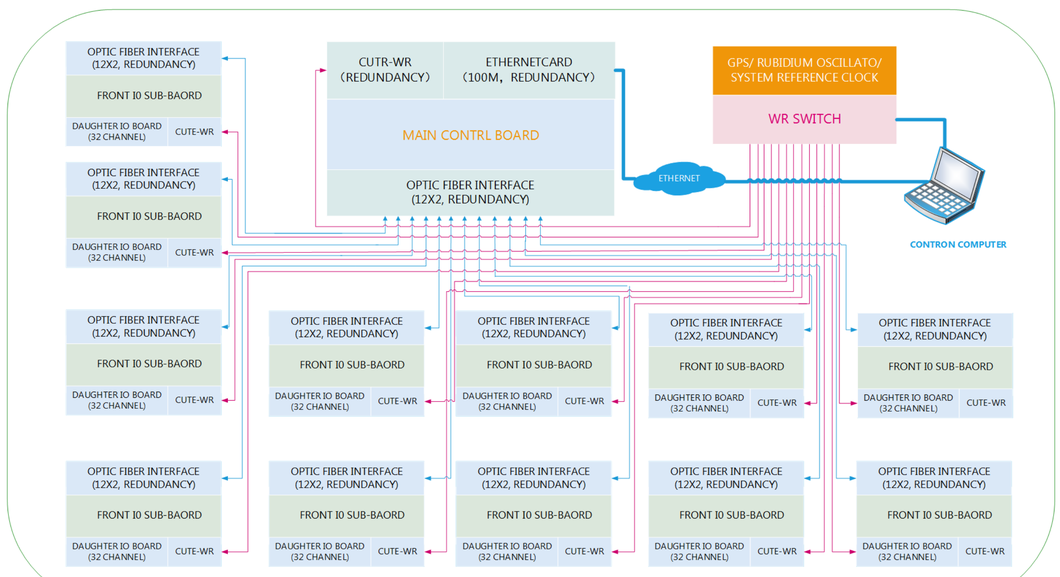
Abstract

In this paper a new fast machine protection system is proposed. This system is designed for the injection I of C-ADS which fault reaction time requires less than 20us, and the one minute down time requires less than 7 times in a whole year. The system consist of one highly reliable control network based on a control board and some front IO sub-boards, and one nanosecond precision timing system using white rabbit protocol. The control board and front IO sub-board are redundant separately. The structure of the communication network is a combination structure of star and tree types which using the 2.5GHz optical fiber links the all nodes. This paper pioneered the use of nanosecond timing system based on the white rabbit protocol to determine the time and sequence of each system failure. Another advantage of the design is that it uses standard FMC and an easy extension structure which made the design is easy to use in a large accelerator.

Fast Machine Protection System

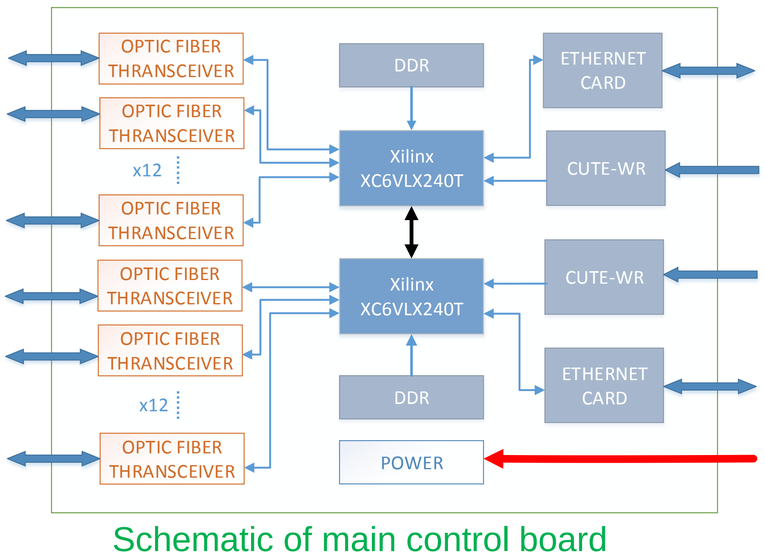
The ADS injection I fast protection system is composed of a main control board, some front IO sub-boards, some supervisory computers and one WR nanosecond precision timing system. Front IO sub-board monitors the 24V or 5V switch signal from the LLRF, PS, Vacuum, RFQ and other critical points. When the monitored points occur error, it sends the error signal to the main control board through optical fiber. The signal contains the time information that is labelled by the White Rabbit system. The main control board analyses and judgments the error through the stored fault tree. Then, it issued the processing results to the front IO sub-boards. Meanwhile, the main control board record the error, process the result and send it to the supervisory computer.



Schematic of fast machine protection system

Main Control Board

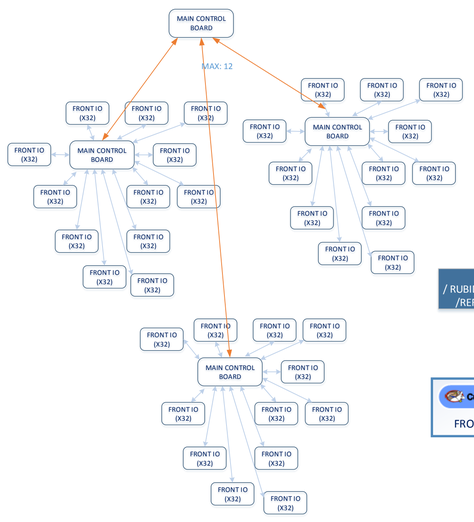
The main control board uses Xilinx XC6VLX240T FPGA. The board can receives12 channel signals from the front IO sub-board. It will complete analysis, feedback, store and send alarm signal function. The status log information will regularly sent to upper computer by a 100Mbps Ethernet sub-card. the main control board also uses redundancy design, including FPGA, optic fiber transceiver, Ethernet and White Rabbit. The double FPGA will timely check the status of each other, and automatically take over the task of the error one.



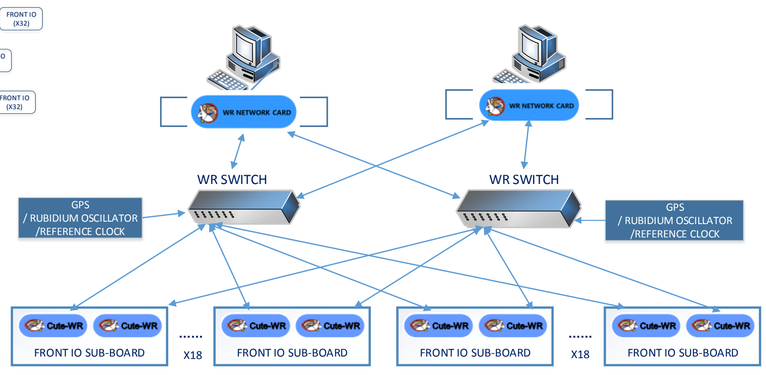
Schematic of main control board

Network Structure

The framework of the network is a star and tree combination structure. A main control board can control 12 block IO sub-board, and an IO sub-board can manage 32 inputs and 32 outputs separately. It will form a 384 nodes network. When we need a greater network, we can link tow subnet. It can reach 4068 nodes. If we want to a much bigger one, we can cascade again.



Schematic of network structure



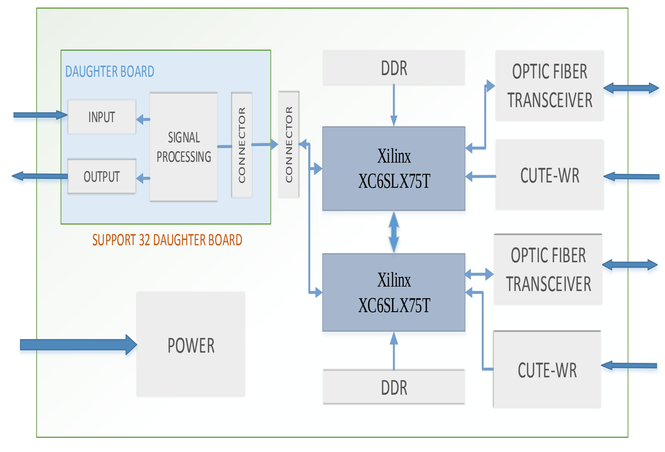
Schematic of WR system

White Rabbit System

The network is composed of a white rabbit switch, some front end Cute-WR modules and a white rabbit protocol network card that responsible for the linking to computer. The Cute-WR module is the terminal module of the system. It can receive clock and time signal from the switch. A switch can link 18 Cute-WR modules. For this system, we use 13 Cute-WR modules, 12 of which are used in the link of 12 front IO sub-boards, and the other for main control board. The entire WR network uses backup design. The minimum time gaps is 8ns.

Front IO Sub-board

The front IO sub-board uses a 2.5U box. It uses the motherboard and daughterboard design. The mother board uses XC6SLX75T-3FGG676I FPGA as the main processor, and communicates with 32 daughterboard through 32 cables. The transmission protocol is Aurora 8B/10B. The line rate is 2.5Gbps. We use watchdog, redundancy FPGA, DDR and optic fiber transceivers to improve our reliability.



Schematic of front IO sub-board

summary

This paper presents a new scheme of accelerator machine protection system. It can make the protection action time less than 20us and it use sub-nanosecond timing system as the clock and time module, which make it possible to determine the errors occur time and the error sequence. And each node of the system is an independent and easy organized one. It made the system with good integration and scalability.