Operation Status of J-PARC Timing System and Future Plan

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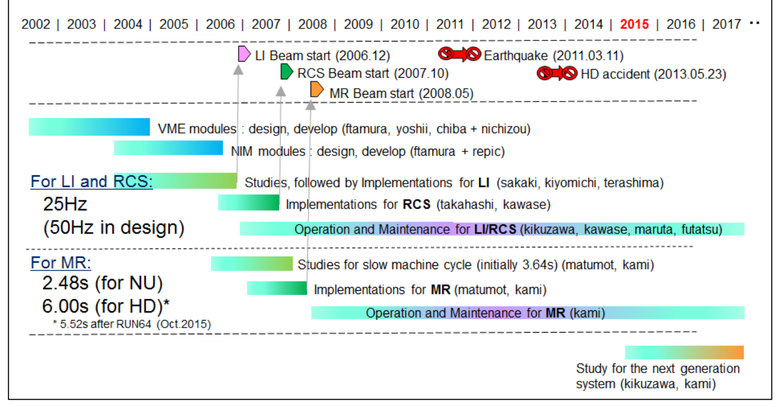
Facts in short

1. J-PARC is an accelerator complex located in Ibaraki, Japan
   1. Rapid cycle: LI(400MeV Linac) and RCS(3GeV) - 25Hz
   2. Slow cycle: MR(30GeV Main Ring) - 2.48s or 6.00s (5.52s after Oct.2015)
2. Hardware
   1. Home-design VME modules for control, NIM modules for signal generation
   2. Base signals (clock, trigger, type-code) are distributed over the facility buildings, using the fiber-optic cable network
3. Software
   1. EPICS and its tools are used in general
   2. Java and python are preferred for table(waveform)-data handlings
4. Scale of the system
   1. One send-module
   2. LI/RCS/MR – 118/43/45 VME receiver-modules, ~540/220/300 endpoints

Summary

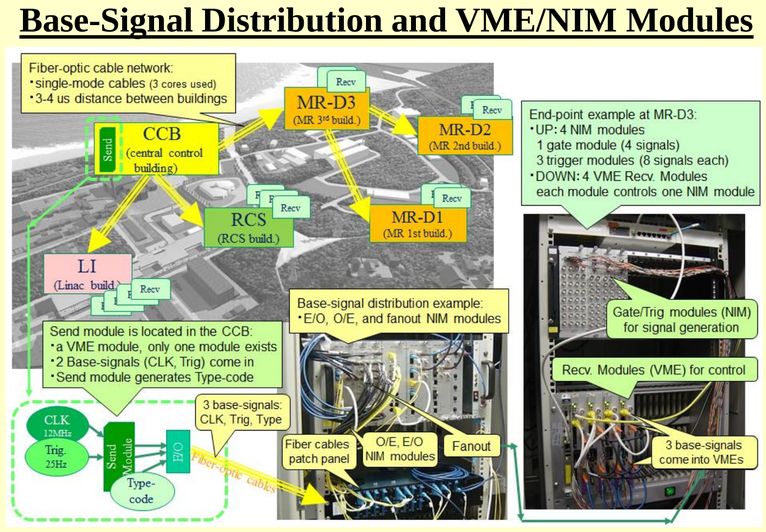
1. J-PARC Timing hardware was developed roughly 10 years before, in collaboration with domestic companies
2. Timing software was developed in house
3. Rapid-cycle and slow-cycle co-exist
4. Since 2006, the timing system has been used successfully in accelerator operation, with good enough reliability
5. We start discussion on possible migration and extension for the next decade

J-PARC timing: History Overview



Timing System Details

Base-Signal Distribution and VME/NIM Modules



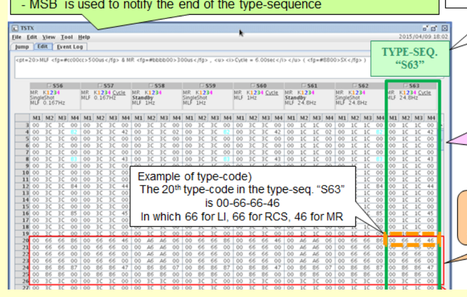
Send module ; type-sequence and type-code

A send module:
- has a type-memory, which consists of 64 type-sequences
- uses one selected type-sequence at a moment
- sends the type-code in the selected type-sequence one-bye-one at the 25Hz trigger rate

One type-sequence:
- can contain 256 type-codes at maximum
- corresponds to one machine-cycle; 62(150) type-codes for 2.48s(6.00s)

One type-code:
- has 4 subsections; M1(MSB+ spare 7bit), M2(8bit for LI), M3(8bit for RCS), and M4(8bit for MR)
- MSB is used to notify the end of the type-sequence

Example of type-sequence)
・The "S63" sequence is for MLF:25Hz+MR:2.48s operation
62 type-codes; consists of 56 for MLF, 4 for MR, 2 empty
・LI(RCS) uses the M2(M3) subsection
- "1C" every 25Hz as a standard shot to MLF
- the 20th to 23rd, "66", are shots to MR injection
- the 24th to 25th , "86", means empty - "no beam"
- the 26th , "3C" , corresponds to a MLF shot with residual magnetic-field corrections caused by the MLF-MR switching magnet
・MR uses the M4 subsection
- every 4 shots (160ms), the code is incremental "41", "42", "43", "44", ...

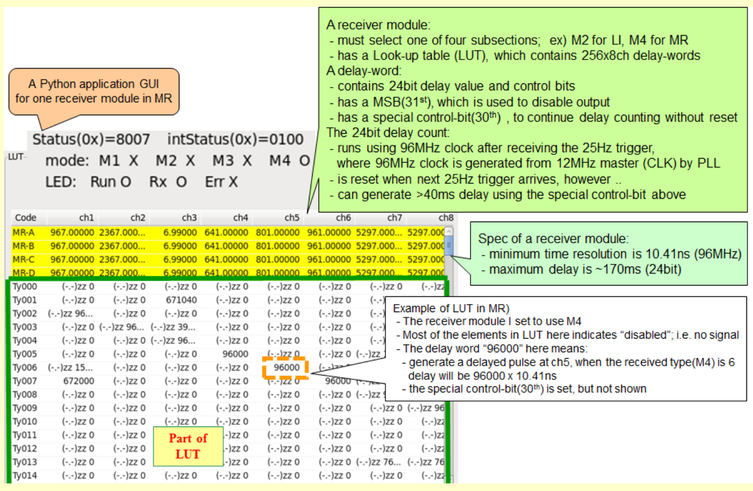


Receiver module ; LUT and delay-word

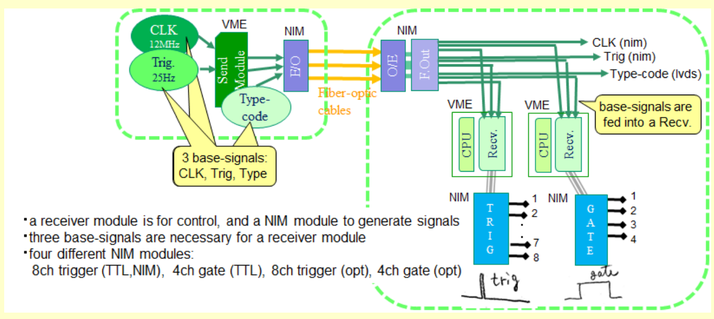
A receiver module:
- must select one of four subsections; ex) M2 for LI, M4 for MR
- has a Look-up table (LUT), which contains 256x8ch delay-words

A delay-word:
- contains 24bit delay value and control bits
- has a MSB(31st), which is used to disable output
- has a special control-bit(30th) , to continue delay counting without reset

The 24bit delay count:
- runs using 96MHz clock after receiving the 25Hz trigger, where 96MHz clock is generated from 12MHz master (CLK) by PLL
- is reset when next 25Hz trigger arrives, however ..
- can generate >40ms delay using the special control-bit above

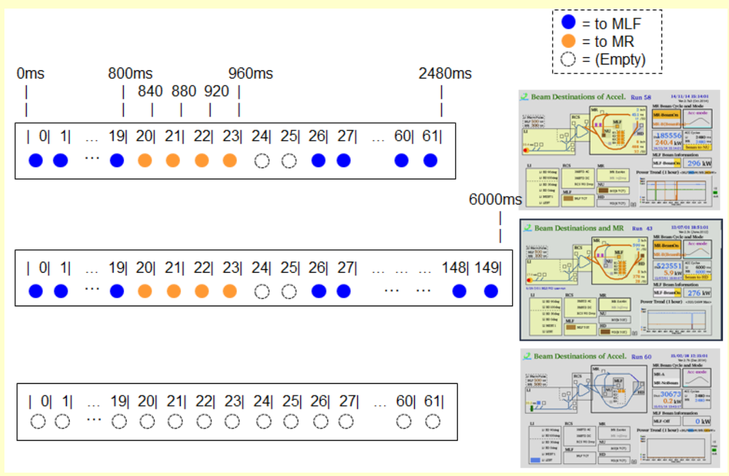


Receiver module, NIM module, and base-signals

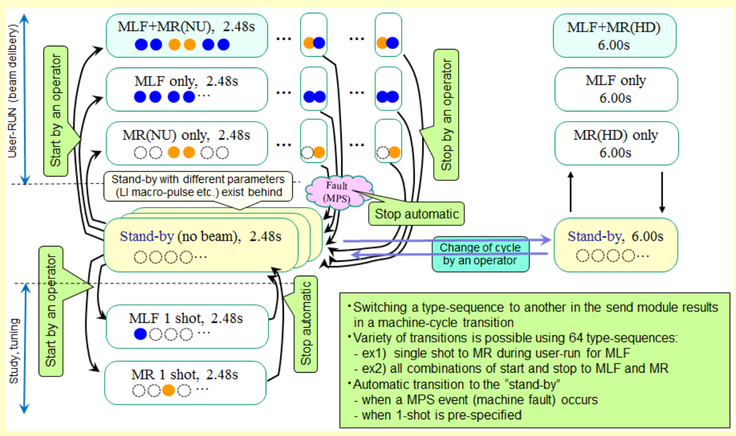


Operation

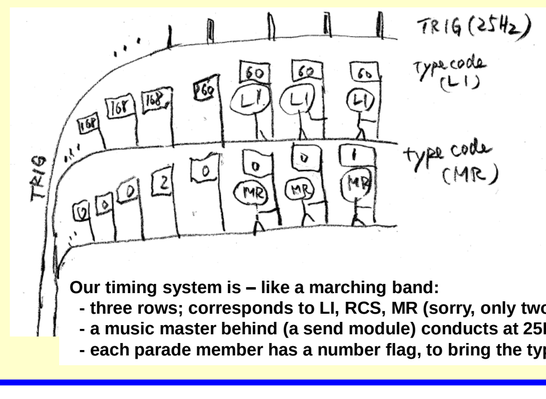
Beam slots in single machine-cycle



Transitions of machine-cycles



Timing Marching Band



Our timing system is – like a marching band:
- three rows; corresponds to LI, RCS, MR (sorry, only two are shown !)
- a music master behind (a send module) conducts at 25Hz beat
- each parade member has a number flag, to bring the type-code to a receiver

Future

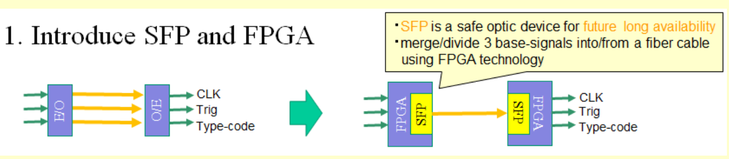
Evaluation of present system

1. Since 2006, VME modules (~200 modules in total) have worked very well without faults, except a few pieces
2. Problems and considerations
   1. Base signals, especially type-codes as a LVDS form, suffer external noise influences from pulsed power-supplies.
   2. Life of optic devices : optic devices used in E/O and O/E modules, made in 2006-2010, are already discontinued
   3. ADS, a new facility in J-PARC, will be constructed. Additional 25Hz beams will be needed around 2018-2019.
   4. No good proposal for small component: when only one delay is requested for a new device, set of a VME system and NIM modules is necessary, results in too much space.

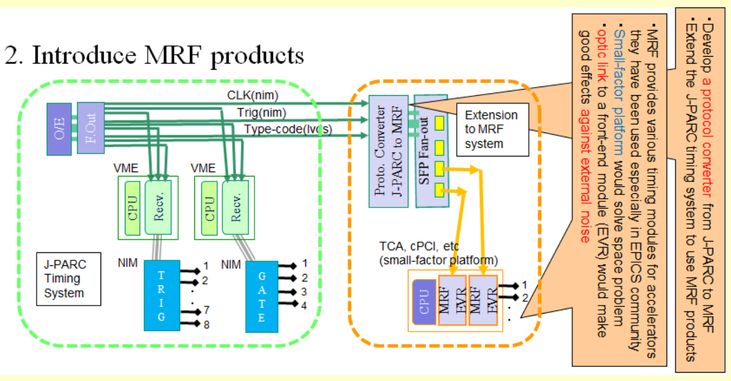
Ideas for the future

- Following ideas have been discussed
- Studies will be made in the near future

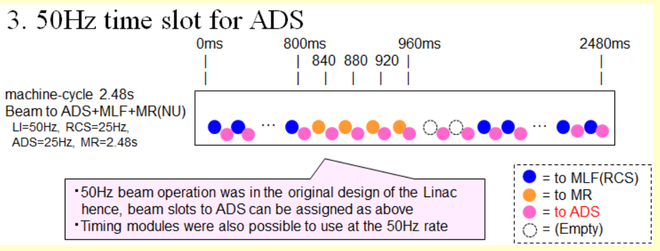
1. Introduce SFP and FPGA



2. Introduce MRF products



3. 50Hz time slot for ADS



Misc. Information

Synchronization timing

・Extraction kicker of RCS must be synchronized with the circulating beams. This trigger is generated by the RCS RF.

・MR injection devices are triggered by the same signal with appropriate delays.

・This delay is generated by a dedicated VME board, with resolution of 2ns.

Daily modulation

・The length of the fiber-optic cables between buildings is about 1 km. One-way path-through time is 3-4 us.

・Daily modulation due to environmental changes was observed: roughly ~1 ns.

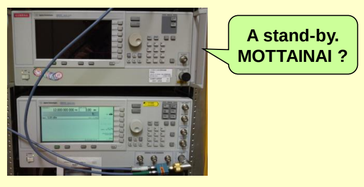
・This modulation is considered small enough and permissible for our timing.

Master oscillator

・The master oscillator is a commercial product, a high-stability function generator.

・It generates the master clock: 12.000,000,000 MHz.

・We always keep a stand-by together, since the master oscillator is indispensable.



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