Commissioning of National Synchrotron Light Source-II (NSLS-II) Fast Orbit Feedback System

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Outline

• NSLS-II status and parameters overview
• NSLS-II orbit feedback system
  • Technical requirements and specifications
  • Hardware review
• Individual eigenmode compensation
  • NSLS-II FOFB algorithm with individual eigenmode compensation
• Implementation
  • FPGA
  • Latency
• Performance measurement
• Summary
**NSLS-II Key performance**

- **Beamline operation started Feb. 2015 with 150 mA**
- **Oct started 250 mA top-off operation**
  - 3 GeV, 500 mA beam current with 1 nm-rad horizontal and 8 pm-rad vertical emittance.
    - Beam sizes at source points are ~100 µm / 3 µm (x/y)
  - High beam stability in position (<10% of rms size) and angle (<10% of rms divergence)
  - 1080 bunches in 1320 RF buckets, 3 hrs lifetime
  - Top off injection for stable intensity (±0.5% variation)

<table>
<thead>
<tr>
<th>Design Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Beam Energy [GeV]</td>
<td>3</td>
</tr>
<tr>
<td>Beam Current [mA]</td>
<td>500</td>
</tr>
<tr>
<td>Circumference [m]</td>
<td>792</td>
</tr>
<tr>
<td>Number of DBA cells</td>
<td>30</td>
</tr>
<tr>
<td>X/Y Emittance [nm-rad]</td>
<td>1/0.008</td>
</tr>
<tr>
<td>Relative energy Spread</td>
<td>0.1%</td>
</tr>
<tr>
<td>RF Voltage [MV]</td>
<td>4.9</td>
</tr>
<tr>
<td>Number of ID straights</td>
<td>15 SSS and 12 LSS</td>
</tr>
</tbody>
</table>

One super-period SR Lattice function

Long ID = 9.3m  Short ID = 6.6m
Slow correctors (Qty=6)
- Slow response – 2 Hz
- Strong strength – 800 μrad
- Utilized for – Alignment
- Slow orbit feedback

Fast correctors (Qty=3)
- Fast response – 2 kHz
- Weak strength – 15 μrad
- Utilized for – Fast orbit feedback

100 mm slow(8)
156 mm slow(4)
30 mm fast (air core)
System Specifications

- Number of CCs : 30 sets
- Minimize beam motion < 10 %
- Feedback rate : 10 kHz
- Bandwidth : ~ 200 Hz
- Control algorithm : SVD, Individual Eigenmode with PID control
  - FPGA based parallel matrix calculation
- Number of BPMs : 180 ea + ID bpms (27)
  - NSLS-II in house designed high performance rf BPM
- Number of a fast correctors : 90 ea
  - 15 urad, 20 bit current output resolution, 1 ppm step response, 2 kHz small signal bandwidth
- Virtex-6 FPGA based hardware digital processor
  - Local cell installed own feedback processor which called Cell Controller unit
- Communication update rate is 10 kHz
  - 5 Gbps fiber optics communication for BPM and CC, 100 Mbps copper for PS
- All System’s (CC/BPM/Al/PS) synchronized with accelerator timing system
Diagnostics/PS Rack and Cell Controller Chassis

- 100 Mbit/s link for corrector setpoints
- IO signals (16 inputs, 12 outputs, 4 Vout) for fast machine protection
- 5 Gigabit/s SDI link for BPM and CC data
- Gigabit Ethernet to EPICS IOC
- Embedded Event Received
- +/- 0.1 degC temperature controller
- IOC
- EVR
- BPMs
- CC and FOFB
- Serial console
- Power Supply Rack
- +/- 0.1 degC temperature controller
60% fill pattern, beam current was limited to an administrative limit of 25 mA, which corresponds to almost full ADC scale.

- TBT (378 KHz) Resolution at 15 mA ~ 700 nm
- FA (10 KHz) Resolution at 15 mA ~ 200 nm

BPM install status (~270)
- Linac – 6
- LTB – 5
- BR - 36
- BTS - 9
- SR – 211, arc (180), ID (27), Injection(4)
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NSLS-II Serial Device Interface (SDI)

- Ring topology method
- BPM and CC 5 Gbps, bidirectional (CW, CCW direction)
- Global 31 nodes
- bpm local nodes (6-13)
- PS 12 nodes (100 Mbps Ethernet PHY)
- Every 10 kHz transfer packets to neighbor cell
- Global packet size is 780 x 4byte (3120 bytes)
- Local packet size is 26 x 4byte (104 bytes)

Lab test configuration before installation (2013.9)

- Tested total 32 nodes
- Confirmed:
  - Timing, communication protocol, IOC...
  - Firmware functionalities
Topology of the FOFB dedicated network

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FOFB Calculation - Compensation for each eigenmode

\[ d_{gold} \rightarrow -e \rightarrow U^T \rightarrow Q(z) \rightarrow \Sigma^{-1} \rightarrow V \rightarrow \theta \]

\[ R = U \Sigma V^T \]

**Diagram**: The diagram illustrates the compensation process for each eigenmode in the FOFB calculation. The flowchart includes nodes for the gold displacement, correction terms, and transformation matrices, leading to the compensated state. The equations and matrices are visualized through graphical representations, including a reverse orbit response matrix, an UlFPGA matrix, eigenvalues, and a V matrix. The diagram is annotated with labels for the matrices and their interconnections, emphasizing the compensation formula.

**U.S. Department of Energy**

**Brookhaven Science Associates**
FOFB Calculation - Compensation for each eigenmode

\[ d_{gold} \rightarrow e \rightarrow U^T \rightarrow Q(z) \rightarrow \Sigma^{-1} \rightarrow V \rightarrow \theta \]

\[ Q(z) = \begin{bmatrix} Q_1(z) & 0 & 0 & 0 \\ 0 & Q_2(z) & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & Q_N(z) \end{bmatrix} \]

\( c_1, c_2, \ldots, c_N \) is the input projections in the eigenspace.

\( Q_1(z), Q_2(z), \ldots, Q_N(z) \) is the compensator for each eigenmode.

We want to prove that \( Q_1(z), \ldots, Q_N(z) \) only change the corresponding eigenmode in eigenspace without affecting other eigenmodes.
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Cell Controller FPGA internal blocks
Block diagram of the feedback calculation

180° = 480°

4 * 45 = 180°

1/S * PI * V

4 stage SUM

Amp to DAC count
Gain = 524287 / 1.25

Level Conversion

PS

DAC

ps out[0]
ps out[1]
ps out[2]; ps out[3]

1 Hz Injection trigger
10 kHz FOB trigger

EVF

15

SR Cell Controller

EVR

x, y

Block diagram of the feedback calculation

U matrix calculation

EigenComp

EigenComp1

EigenCompSum

1/S * PI * V

4 stage SUM

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FPGA internal layout for FOFB calculation

U^T or R^{-1}

Global X, Y

position [0.239[420][479]

SDI global [0.779]

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x, y
Block diagram of the feedback calculation

U matrix calculation

\[ \mathbf{U} \]

Eigenvector calculation

\[ \mathbf{E} \]

\[ \mathbf{Q}(z) = \mathbf{U}^{-1} \mathbf{Q} \]

\[ \mathbf{V} = \mathbf{U}^T \]

Accelerator

\[ \mathbf{R} = \mathbf{U} \Sigma \mathbf{V}^T \]
Overall timing estimation

- Local BPM data (2.2 us, 104 byte, 5 Gbps, @ 125 MHz)
- Global BPM data transfer link (20 us, 3120 byte, 5 Gbps, @ 125 MHz)
- Calculation (48 us @ 50 MHz, 45x4=180 480 and 540 * 6 matrix calculation)
- Corrector setting (7 us, 100 Mbps @ 25 MHz)
BPM/CC/PSI Hardware Latency measurement

**RF Signal Generator**

- $f_{RF} = 499.680 \, MHz$
- $f_{rev} = 378 \, kHz$

**EVG/EVR Timing**

- 4 way split

**BPM**

- PLL
- EVR

**Cell Controller**

- 5 Gbps GTX
- 10 Gbps Ethernet
- 16 Mbps Fiber

**PSC**

**PSI**

- 20-bit DAC
- Analog reference +/- 10V

**Corrector PS**

**Signal Measurement Scope**

1. RF
2. Tx trigger 100 us
3. CC DAC OUT
4. PSI DAC OUT

BPM Position data
BPM/CC/PSI Hardware Latency measurement

System Transfer function measurement (PS \rightarrow \text{corrector M} \rightarrow \text{chamber} \rightarrow \text{bpm button}) \quad H : 1 \text{ kHz}, \quad V : 800 \text{ Hz}

\[ \text{f}_{RF} = 499.680 \text{ MHz} \]

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RF

Tx trigger 100 us

CC DAC OUT

PSI DAC OUT
BPM/CC/PSI Hardware Latency measurement

System Transfer function measurement (PS -> corrector M -> chamber -> bpm button)  H : 1 kHz,  V : 800 Hz

Signal Measurement Scope

- Fast corrector transfer function, FH1G1C16A
- BPM Position data

**RF**
- Tx trigger 100 us

**PSI DAC OUT**

**CC DAC OUT**

**Trig (10 kHz)**

**System Parameters**
- f_{RF} = 499.680 MHz
- f_{rev} = 378 kHz
- 2.5 Gbps
- 5 Gbps GTX
- 100 Mbps Ethernet
- 16 Mbps Fiber
- Analog reference +/- 10V
- 20-bit DAC

**Additional Notes**
- System Transfer function measurement (PS -> corrector M -> chamber -> bpm button)  H : 1 kHz,  V : 800 Hz
- BPM Position data
PSD/RMS beam motion measurement

Integrated RMS motion in frequency range 1-500Hz, plotted for 12 BPMs in one super-cell (C02 and C03).

180 BPMs, 16384 points of FFT
Average PSD excluding dispersive BPMs, 40 Eignemode, Ki=0.25, Kp=0.5

⇒ With FOFB on, RMS motions in both H and V plane meet the specifications (dashed lines).
Top-off injection mode test

Without feedback

< 1 %

With feedback

1 %
Summary

- Run FOFB user operation since May 2015
- The long term drift was less than 4 um(H) / 1 um(V) during 15 hours.
- BPM SA data shows the orbit stability was improved a factor of 7 to 10.
- BPM FA data shows the noise suppression up to 400 Hz.
- The integrated orbit noise is less than 10 % of beam size.

- Measured open loop system transfer function and system latency
- Run top-off injection mode at 250 mA operation

- Continues study that optimization and operation procedure
Thank you for your attention!

Questions and comments are welcome.
Acknowledgments

• BPM/ Cell controller development :
  Kurt Vetter
  Joseph Mead
  Alfred Dellapenna
  Joseph De Long
  Om Singh

• PSC and PS design:
  Wing Louie
  John Ricciardelli
  George Ganetis